

Amendments of the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the above-identified patent application.

Listing of Claims

1. (Canceled)

2. (Canceled)

3. (Currently Amended) ~~The loop circuit of claim 2 wherein:~~ A phase-locked loop circuit having an input terminal for receiving a reference signal and an output terminal for outputting an output signal locked to
5 said reference signal, and comprising:
a compensation component comprising an oscillator for producing said output signal;
a high-gain coarse feedback path feeding
10 said compensation component, said high-gain coarse feedback path accepting as inputs a reference frequency of said reference signal and an output frequency of said output signal, and causing said compensation component to drive said output frequency to within a predetermined
15 variance from said reference frequency, wherein said coarse feedback path comprises:
a frequency detector having inputs connected to said input terminal and said output terminal, said frequency detector producing a coarse-adjust signal based on a difference between said output frequency and
20 said reference frequency, and
a high-gain signal modifier downstream of said frequency detector; and
a low-gain fine feedback path feeding said compensation component, said low-gain fine feedback path
25 accepting as inputs said reference frequency and said output frequency, and causing said compensation component to drive said output to a phase-frequency lock with said

reference frequency after said coarse feedback path has
caused said compensation component to drive said output
30 frequency to within said predetermined variance from said
reference frequency, wherein said fine feedback path
comprises:

a phase-frequency detector having inputs
connected to said input terminal and said output terminal,
35 said phase-frequency detector producing a fine-adjust
signal based on said difference between said output
frequency and said reference frequency, and

a low-gain signal modifier downstream of
said phase-frequency detector.

4. (Original) The loop circuit of claim 3
wherein:

said oscillator is a current-controlled
oscillator;

5 said low-gain signal modifier is a voltage-
to-current converter having a first gain; and

said high-gain signal modifier is a
voltage-to-current converter having a second gain greater
than said first gain.

5. (Original) The loop circuit of claim 4
wherein said second gain is twenty times said first gain.

6. (Original) The loop circuit of claim 3
wherein:

each of said high-gain signal modifier and
said low-gain signal modifier has a respective gain; and

5 said gain of said high-gain signal modifier
is ten times said gain of said low-gain signal modifier.

7. (Original) The loop circuit of claim 3
further comprising a control circuit adapted to disable
said fine feedback path until said coarse feedback path is
locked and to enable said fine feedback path after said
5 coarse feedback path is locked.

8. (Original) The loop circuit of claim 3 wherein said frequency detector is programmable for user adjustment of said predetermined variance.

9. (Original) The loop circuit of claim 8 wherein said frequency detector comprises:

a reference counter clocked by said reference frequency;

5 a feedback counter clocked by said output frequency;

at least one programmable register programmably storing a respective counter value;

a reference comparator that compares said 10 reference counter to said respective counter value;

a feedback comparator that compares said feedback counter to said respective counter value; and

combining circuitry that (a) when said reference counter reaches said respective counter value 15 before said feedback counter, generates a control signal to increase said output frequency, and (b) when said feedback counter reaches said respective counter value before said reference counter, generates a control signal to decrease said output frequency.

10. (Original) The loop circuit of claim 9 wherein:

said at least one programmable register consists of one programmable register; and

5 said reference comparator and said feedback comparator respectively compare said reference counter and said feedback counter to a single counter value in said one programmable register.

11. (Original) The loop circuit of claim 9 wherein:

said at least one programmable register comprises two programmable registers, a first one of which

5 corresponds to said reference counter and a second one of
which corresponds to said feedback counter; and
said reference comparator and said feedback
comparator respectively compare said reference counter and
said feedback counter to respective counter values in said
10 first and second programmable registers.

12. (Original) The loop circuit of claim 11
wherein said respective counter values in said first and
second programmable registers are equal to one another.

13. (Original) The loop circuit of claim 11
wherein said respective counter values in said first and
second programmable registers are different from one
another.

14. (Original) The loop circuit of claim 9
wherein said combining circuitry comprises:

a detector having as inputs outputs of said
reference comparator and said feedback comparator, said
5 detector producing a latch signal when either of (a) said
reference comparator, and (b) said feedback comparator,
produces an output indicative of one of said reference
counter and said feedback counter reaching its respective
counter value stored in said at least one register;
10 a reference latch and a feedback latch that
respectively latch values in said reference counter and
said feedback counter when said detector produces said
latch signal; and
a subtractor that subtracts the value in
15 said feedback latch from the value in said reference
latch.

15. (Original) The loop circuit of claim 14
wherein said detector comprises an OR gate.

16. (Original) The loop circuit of claim 14
wherein said combining circuitry further comprises:

a programmable offset generator that generates an offset signal; and

5 an adder for combining said offset signal with said control signal.

17. (Original) The loop circuit of claim 3 wherein said coarse feedback path further comprises a digital-to-analog converter between said frequency detector and said high-gain signal modifier.

18. (Original) The loop circuit of claim 3 wherein said fine feedback path further comprises a charge pump and loop filter between said phase-frequency detector and said low-gain signal modifier.

19. (Currently Amended) The loop circuit of claim [[2]]3 further comprising an output scaling counter downstream of said output terminal.

20. (Currently Amended) The loop circuit of claim [[2]]3 further comprising an input scaling counter upstream of said input terminal.

21. (Currently Amended) The loop circuit of claim [[2]]3 further comprising a feedback scaling counter between said output terminal and each said feedback path.

22. (Currently Amended) ~~The loop circuit of claim 1 wherein:~~

~~said loop circuit is a delay locked loop,~~
~~said compensation component comprises a~~
5 ~~controlled delay line for producing a phase delayed output signal;~~

~~said reference signal has an input phase,~~
~~said output signal has an output phase; A~~
delay-locked loop circuit having an input terminal for
10 receiving a reference signal and an output terminal for
outputting an output signal locked to said reference
phase, and comprising:

a compensation component comprising a
controlled delay line for producing said output signal,
15 wherein said output signal is phase-delayed;
said a high-gain coarse feedback path
feeding said compensation component, said high-gain coarse
feedback path accept[[s]]ing as inputs said reference
signal and said output signal, and caus[[es]]ing said
20 controlled delay line to drive said an output phase of
said output signal to within [[said]]a predetermined
variance from [[said]]an input phase of said reference
signal; and
said a low-gain fine feedback path feeding
25 said compensation component, said low-gain fine feedback
path accept[[s]]ing as inputs [[said]]a reference
frequency of said reference signal and [[said]]an output
frequency of said output signal, and caus[[es]]ing said
controlled delay line to drive said output signal to a
30 phase lock with said reference input signal after said
coarse feedback path has caused said controlled delay line
to drive said output phase to within said predetermined
variance from said input phase.

23. (Currently Amended) The loop circuit of
claim 22 wherein:

said coarse feedback path comprises:
a first phase detector having inputs
5 connected to said input terminal and said output terminal,
said first phase detector producing a coarse-adjust signal
based on a difference between said output phase and said
input phase, and
a high-gain signal modifier downstream of
10 said phase detector; and
said fine feedback path comprises:
a second phase detector having inputs
connected to said input terminal and said output terminal,
said second phase detector producing a fine-adjust signal
15 based on said difference between said output phase and
said input phase, and

a low-gain signal modifier downstream of said second phase detector.

24. (Original) The loop circuit of claim 23 wherein:

said controlled delay line is a current-controlled delay line;

5 said low-gain signal modifier is a voltage-to-current converter having a first gain; and

said high-gain signal modifier is a voltage-to-current converter having a second gain greater than said first gain.

25. (Original) The loop circuit of claim 24 wherein said second gain is twenty times said first gain.

26. (Original) The loop circuit of claim 23 wherein:

each of said high-gain signal modifier and said low-gain signal modifier has a respective gain; and

5 said gain of said high-gain signal modifier is ten times said gain of said low-gain signal modifier.

27. (Original) The loop circuit of claim 23 further comprising a control circuit adapted to disable said fine feedback path until said coarse feedback path is locked and to enable said fine feedback path after said
5 coarse feedback path is locked.

28. (Original) The loop circuit of claim 23 wherein said phase detector is programmable for user adjustment of said predetermined variance.

29. (Original) The loop circuit of claim 23 wherein said coarse feedback path further comprises a digital-to-analog converter between said phase detector and said high-gain signal modifier.

30. (Original) The loop circuit of claim 23 wherein said fine feedback path further comprises a charge

pump and loop filter between said phase detector and said low-gain signal modifier.

31. (Currently Amended) The loop circuit of claim [[1]]3 wherein said predetermined variance is programmable.

32. (Currently Amended) A programmable logic device comprising the loop circuit of claim [[1]]3.

33. (Original) A digital processing system comprising:

processing circuitry;
a memory coupled to said processing
5 circuitry; and
a programmable logic device as defined in claim 32 coupled to the processing circuitry and the memory.

34. (Original) A printed circuit board on which is mounted a programmable logic device as defined in claim 32.

35. (Original) The printed circuit board defined in claim 34 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic
5 device.

36. (Original) The printed circuit board defined in claim 35 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

37. (Currently Amended) An integrated circuit device comprising the loop circuit of claim [[1]]3.

38. (Original) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing
5 circuitry; and
an integrated circuit device as defined in
claim 37 coupled to the processing circuitry and the
memory.

39. (Original) A printed circuit board on which
is mounted an integrated circuit device as defined in
claim 37.

40. (Original) The printed circuit board
defined in claim 39 further comprising:
memory circuitry mounted on the printed
circuit board and coupled to the integrated circuit
5 device.

41. (Original) The printed circuit board
defined in claim 40 further comprising:
processing circuitry mounted on the printed
circuit board and coupled to the memory circuitry.

42. (New) The loop circuit of claim 22 wherein
said predetermined variance is programmable.

43. (New) A programmable logic device
comprising the loop circuit of claim 22.